	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	15	((CMOS OFFSET PHASE LOCK LOOP OR CMOS OFFSET PLL LOOP) AND (CMOS SUBSTRATE)) AND (CMOS ADJ PHASE ADJ LOCK ADJ LOOP)	USPAT	2004/04/12 14:20
2	BRS	L2	43610	455/$.CCLS.	USPAT	2004/04/12 14:30
3	BRS	L3	22321	331/$.CCLS.	USPAT	2004/04/12 14:30
4	BRS	L4	63369	2 OR 3	USPAT	2004/04/12 14:31
5	BRS	L5	23689	4 AND (CMOS PHASE LOCK LOOP)	USPAT	2004/04/12 14:31
6	BRS	L6	2022	5 AND (PHASE ADJ LOCK ADJ LOOP)	USPAT	2004/04/12 14:32
7	BRS	L7	781	6 AND OSCILLATOR AND MIXER	USPAT	2004/04/12 14:32
8	BRS	L8	391	7 AND (PHASE ADJ DETECTOR)	USPAT	2004/04/12 14:33
9	BRS	L9	170	8 AND (ERROR ADJ SIGNAL)	USPAT	2004/04/12 14:34
10	BRS	L10	55	9 AND (VCO OR VOLTAGE CONTROLLED OSCILLATOR) AND (BANDPASS ADJ FILTER)	USPAT	2004/04/12 14:35
11	BRS	L11	14	10 AND CMOS	USPAT	2004/04/12 15:44
12	BRS	L13	1	12 and (tunable adj oscillator)	USPAT	2004/04/12 15:46
13	BRS	L12	55	10 and (phase adj lock adj loop)	USPAT	2004/04/12 16:05